REMARKS

Applicants appreciate the Examiner's acknowledgment of the claim for priority under 35 USC 119.

Submitted herewith is a certified copy of the corresponding Japanese patent application (JP 2000-067141, filed March 7, 2000). An indication that this document has been safely received would be appreciated.

The documents referenced in the Information Disclosure Statement filed on August 15, 2000 were mentioned in the specification. That is, the required concise statement of relevance for each of the documents is provided in the specification, which is permitted. Therefore the documents should be considered by the Examiner. A copy of the PTO-1449 Form is attached. The Examiner is requested to initial and return a copy of the PTO-1449 Form to the undersigned to indicate that the documents listed thereon were considered by the Examiner.

The present invention relates to a radio frequency identification (RFID) that uses dynamic impedance variation by such means as intermittent load operation for communication to an external apparatus as defined in ISO 10536 and ISO 14443. In the conventional RFID, a hysteresis power-on-reset circuit configuration is adopted in which the reset voltage is set at

a working guarantee voltage level and the sum of the reset voltage and a voltage drop due to a dynamic load variation is used as a reset release voltage. That is, the hysteresis circuit configuration is of a two-state type and the foregoing condition causes a reduction in the working voltage margin of the IC.

According to the present invention, the RFID has inner elements or a semiconductor integrated circuit that is put in an active state from a reset state (non active state) when it is detected that a level of the DC voltage, attained by rectifying an AC wave induced on the antenna, is higher than a reset release voltage level, and maintains a state of impedance of the semiconductor integrated circuit at a low impedance state in the case of the reset state. That is, the semiconductor integrated circuit has two states of impedance, a high impedance state and a low impedance state, as opposed to a conventional RFID, which has a high impedance state that is maintained even in the case of the reset state. Further, according to the invention, the RFID uses a simple configuration of the power-on-reset circuit and obtains a maximum working voltage range since the reset release voltage can be equal or nearly equal to the reset voltage. See page

8, lines 3-8 of the specification, as well as page 13, lines 11-22 and page 14, lines 9-10 thereof.

The claims have been amended to clearly set forth that which the Applicants regard as the invention. The claims stand rejected as being anticipated under 35 U.S.C. § 102(b) by Carroll, U.S. Patent No. 4,857,893 or by Beigel, U.S. Patent No. 4,333,072. Reconsideration of the rejections is requested for the following reasons.

In Carroll, the invention is directed to a small, inexpensive and reliable transponder device on a single chip by using the diodes both as a rectifier circuit and a balance modulator circuit. See, col. 3, lines 11-20 and 58-60 of the reference. However, Carroll does not disclose first means for powering a transponder upon detection of a condition that the voltage attained by rectifying an alternating current (AC) wave induced on antenna 20 is higher than a predetermined voltage level.

In the present invention, the power-on-reset circuit 7 outputs a power-on-reset signal for placing the circuit in an active state when a DC power supply voltage reaches a predetermined reset release voltage level (see the specification, page 12, lines 5-8). On the other hand, in Carroll, the operating power of the DC supply voltage from the

rectifier 22 is distributed to the circuits over power lines 36 and 38 (see col. 6, lines 38-44 of the reference). The circuits (CMOS) need a supply voltage (VDD) maintained at a prescribed level only when the circuits are active (i.e., drawing current). Whether the elements are in an active state or a non-active state is determined by the power-on-reset signal, according to the present invention.

The Office Action states that Carroll can be interpreted to show that a bridge circuit controls the impedance state of transponder 14, citing page 3, lines 13-14 of the Office Action. Further, it is stated that this implies that the data transmission of the transponder 14 is controlled by its state of impedance. However, Carroll does not suggest that the bridge circuit controls the impedance state of transponder 14 and that the data transmission of the transponder is controlled by its state of impedance. Data transmission is performed by an impedance variation, in which alternate states of the high impedance state and the low impedance state, of the bridge circuit with NAND gate 68 and of the FETs 9 and 10, as well as resistors 11, 12 with the modulator 63. Further, it is not necessary for the impedance of transponder 14 to be high in order for the transponder to transmit.

The Office Action further states that "it is inherent that Zener diode 66 turns off and places transponder 14 in a reset state or low impedance state when the applied DC voltage is lower than the threshold voltage or avalanche voltage of the Zener diode 66. (See page 3, lines 21-23 of the Office Action.) However, Carroll does not suggest that the Zener diode 66 puts transponder 14 in a reset state or low impedance state. A Zener diode has a very low impedance when the applied voltage is higher than the threshold voltage and a very high impedance, that is almost in an open state, when the applied voltage is lower than the threshold voltage. Therefore, the Zener diode is used only for stabilizing the voltage (VDD), as discussed in col. 7, lines 67-68 of the reference. The Zener diode in the open state has no action and cannot place transponder 14 in a reset state or low impedance state.

Further, Carroll does not disclose or suggest the subject of preventing a re-reset action performed at the time of voltage drop due to impedance variation as a method of communication after release of reset. Therefore, Carroll neither discloses nor suggests the present invention, such as maintaining a state of impedance of the semiconductor

integrated circuit at a low impedance state in case of the reset state, as claimed by Applicants.

With respect to claims 5-8, the Examiner mentions that the rectifier/balanced modulator circuit 22 is equivalent to the power-on-reset means claimed by Applicants by citing col. 11, lines 11-27 of the reference. However, there is no description of the power-on-reset means in the cited passage of the reference. The power-on-reset means corresponds to the power-on-reset circuit 7 of the present invention. There is no equivalent circuit shown by Carroll. Therefore, the rejection based on Carroll should be withdrawn.

With respect to the rejection of the claims as being anticipated by Beigel, Applicants disagree with the interpretation given to the reference. Specifically, the Beigel reference is relied upon for showing a capacitor 71, diode 73 and Zener diode 77 that form a first means for releasing a reset state or power-on-reset means. However, the Zener diode 77 is used for stabilizing the DC voltage and also for protecting the logic circuitry against overload caused by high voltage. See col. 6, lines 21-25 of the reference. Therefore, the power-on-reset means as claimed by Applicants differs from the combination of the capacitor, diode and Zener diode 77 of Beigel.

Further, Beigel discloses a circuit 83 which is controlled by the count value of circuit 81 and is employed as a variable load on the coil 65 as set forth in col. 6, lines 26-62 of the reference. However, the count value is not defined when the DC voltage is supplied and no determination is made whether the impedance of the load is high or low. See, col. 9, lines 40-41 of the reference.

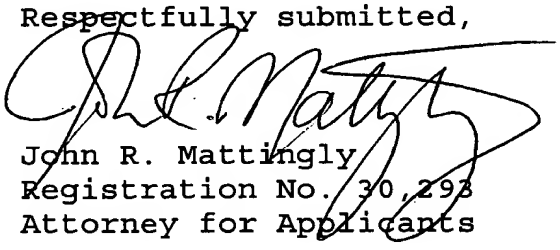
In claim 1, Applicants set forth that the impedance is maintained at the low impedance state in the reset state, and similarly in claim 4, the impedance is claimed as being decreased to a low state in the reset state. Claim 6 includes that when a voltage is applied to the power-on-reset means that is lower than a threshold level, the impedance of the IC device is maintained at a low state. Further, as set forth in claim 8, when a voltage is applied to the power-on-reset means that is lower than a threshold value, the impedance of the integrated circuit element is maintained at the lowest state. Beigel does not disclose these elements of the claimed combination set forth by Applicants.

With respect to claim 10, Beigel does not disclose that when a voltage is applied to the power-on-reset means that is lower than a threshold level, a terminal of the load resistor having another terminal connected with a terminal of a coil of

the antenna is connected to a ground potential through a switching element, as claimed. Therefore, the claims are not anticipated by Beigel, and the 35 U.S.C. § 102(b) rejection should be withdrawn.

In view of the foregoing amendments and remarks, reconsideration and reexamination are respectfully requested.

Respectfully submitted,



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